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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/759,936
Filing Date: January 16, 2004
Appellant(s): CHAUDHRY ET AL.

Gregory W. Carr
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed October 22, 2007, appealing from the Office action mailed May 18, 2007.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct. However, the rejections of claims 1-24 under 35 U.S.C. 112, first paragraph, have been withdrawn by the Examiner. Accordingly, this appeal only involves claims 1-24 rejected under 35 U.S.C. §103(a).

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

B. Whether Claims 1-24 are patentable over Radjassamy in view of Lim.

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner.

A. Whether Claims 1-24 are sufficiently enabled in the Application.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

2004/0186703	RADJASSAMY	9-2004
5,481,209	LIM ET AL.	1-1996

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

A. Claims 1-24 are rejected under 35 U.S.C. 103(a) as being unpatentable over Radjassamy, U.S. Patent Application Publication No. 2004/0186703 A1 Published September 23, 2004, and filed March 20, 2003, in view of Lim et al., U.S. Patent 5,481,209 issued January 2, 1996.

A-1. Regarding claim 1, Radjassamy discloses a method for approximating power consumption of a circuit with plurality of local clock buffers (LCBs), comprising:

inputting a Hardware Descriptive Language (HDL) simulator data of the circuit (The HDL language environment provides a design, simulation, and synthesis platform, paragraph [0015]);

inputting net capacitance data of the circuit (as shown in FIG. 4, capacitance are associated with various power consumption components as capacitors);

inputting energy model data (power consumption equation P_{EST}, for power consumption component models shown in FIG. 5A-5F); and

generating power consumption data from the HDL simulator data, the capacitance data, and the energy model data (the power consumption of the entire sub-block may be estimated, paragraph [0086]).

storing, for subsequent use, an operational model based on the generated power consumption data (Schematic editors produce various data and file types, such as model files 208, paragraph [0017]).

Radjassamy fails to expressly disclose wherein the energy model data further comprises extrapolating energy data by [increasing or] decreasing the number of active LCBs. Nevertheless, Radjassamy discloses at paragraph [0018], "the reduction factor represents a composite probabilistic activity profile associated with each power consumption component that is based on its structural, functional, design and process constraints. Using the *reduction factors for each sub-block*, sub-block level, or portion of the IC of interest, the modified netlist generator 217 provides a modified netlist that *uses a reduced number of components* (e.g., FETs, flip-flops, and the like) to model the portion of the IC of interest as illustrated in further detail in FIG. 4 hereinbelow. Subsequently, the power estimation engine 216 estimates the power consumption based on the modified netlists at the appropriate circuit level, which is essentially a function of a power factor that is modulated by the reduction factors." Using the equation at paragraph [0048] as an example, wherein "F represents the reduction factor for the flip-flops" (paragraph [0055]). "The reduction factor incorporates design-based activity profiles of the flip-flops and may represent a coefficient between 0 and 1 that corrects the worst-case power by taking into considerations such as clock toggling rate and flip-flop toggling rates (paragraph [0056]). It is well-known that the flip-flops will not change state and will consume minimum power when the

clock toggling rate is zero (i.e., clock is inactive). In other words, taking into considerations of clock toggling rate when it is zero, the reduction factor becomes zero representing minimum power consumption of the corresponding flip-flops in a sub-block. Furthermore, Radjassamy suggests that each sub-block may apply its own reduction factor (i.e., taking into considerations of clock toggling rate for each individual sub-block). Therefore, via the "reduction factors" of the power consumption equations P_{EST} (energy model), Radjassamy's estimated power consumption of an integrated circuit does comprise extrapolating energy data by the number of active sub-blocks (i.e., the clock toggling rate is not zero). However, Radjassamy still fails to expressly disclose each clock toggling rate to be zero or non-zero may be accomplished via the inactive or active LCBs.

Lim et al. disclose an apparatus and method for improved clock distribution and control in an integrated circuit having the ability to selectively inhibit clock signals at the local buffer 46. Using inhibit 52 to inhibit the clock at selected locations of the integrated circuit 10 allows for reduction of power dissipation (column 4, lines 62-67). Other features include locally buffered clock signals and multiple clock enables (column 3, lines 33-35). The advantages include reduced delay between buffers and reduced skew across a tributary (column 3, lines 40-42). In other words, Lim et al. suggest power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-blocks as well as clock skew across a tributary may be reduced by using a local clock buffer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the reduction factors of the power consumption equations P_{EST} taught by

Radjassamy to incorporate the number of inhibited clock signals at local buffers taught by Lim et al. because, as suggested by Lim et al., power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-blocks as well as clock skew across a tributary may be reduced by using a local clock buffer.

A-2. Regarding claim 2, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

A-3. Regarding claim 3, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraphs [0067] and [0086]).

A-4. Regarding claim 4, Radjassamy further discloses wherein the method further comprises inputting template data, wherein the template data is at least configured to contain relative power consumption data for each LCB of the plurality of LCBs (as shown in FIG. 5A-5C and 5E-5F, each of the various power consumption components may have its own clock input).

A-5. Regarding claim 5, Radjassamy further discloses wherein the relative power consumption data of each LCB of the plurality of LCBs are at least configured to be the same [or different] (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

A-6. Regarding claim 6, Radjassamy further discloses wherein each LCB of the plurality of LCBs is at least configured to consume the same amount of power (for example, I_i represents the current of clock type i, paragraph [0044]; same current for same clock type).

A-7. Regarding claim 7, Radjassamy further discloses wherein the energy model data further comprises extrapolating energy data by increasing or decreasing numbers of active input signals to the circuit (for example, activity factors, paragraphs [0067] and [0086]).

A-8. Regarding claim 8, Radjassamy further discloses wherein the generating power consumption data is at least configured to utilize the template data (the power consumption of the entire sub-block may be estimated by aggregating the power consumption estimates of its constituent power consuming components, paragraph [0086]).

A-9. Regarding claims 9-16, these apparatus claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

A-10. Regarding claims 17-24, these computer program product claims include equivalent method limitations as in claims 1-8 and are unpatentable using the same analysis of claims 1-8.

(10) Response to Argument

1. The Form and Content of the Examiner's Rejections under Section 112, First Paragraph, Were Improper and Insufficient

1-1. Appellants argue:

"Applicants respectfully submit that the Examiner has failed to meet his burden as required under the M.P.E.P. Further, Applicants respectfully submit that even had the Examiner applied the appropriate test, the Claims as amended are supported by the disclosure in such a way as to satisfy the requirements of Section 112, first paragraph." (page 11, paragraph 2, Appeal Brief)

Appellants' argument is persuasive. The rejections of claims 1-24 under 35 U.S.C. 112, first paragraph, in Office Action dated May 18, 2007, have been withdrawn.

2. The Form and Content of the Examiner's Rejections under Section 103 Were Improper and Insufficient

2-1. Appellants argue:

"Specifically, Applicants respectfully note that the examiner offers Lim as showing "inhibiting the clock at selected locations" to allow for "reduction of power dissipation." But the Examiner cannot show anywhere in Lim where Lim even hints at "reduced estimation of power dissipation." Instead, Lim teaches using LCBs to reduce actual power dissipation, not an estimated power dissipation, and certainly not "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Lim expressly teaches, "Inhibiting the clock at selected locations of the integrated circuit allows for reduction of power dissipation, and specific logical operations involving only part of the integrated circuit chip logic." Lim, col. 3, lines 19-22. Nowhere does Lim come anywhere close to teaching, "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims." (page 13, paragraph 1, Appeal Brief)

The Examiner respectfully disagrees with the Appellants' argument.

As noted by Appellants, Lim expressly teaches, "Inhibiting the clock at selected locations of the integrated circuit allows for reduction of power dissipation, and specific logical operations involving only part of the integrated circuit chip logic." (column 3, lines 19-22) In other words, Lim et al. suggest power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-clocks.

Furthermore, Lim et al. disclose, "Design of complex integrated circuits is accomplished by computer simulation which allows the integrated circuit designer to easily implement and test his design before committing it to silicon." (column 3, lines 33-36) Therefore, Lim's teachings have most likely been verified by simulation. In other words, Appellants' argument regarding Lim, has not even hinted at "reduced estimation of power dissipation" is not persuasive. Appellants' argument against the references individually is also not persuasive because one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.*, 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986). As detailed in section **2-2** below, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Radjassamy and Lim et al. not only because they both are in the same endeavor to relate the power consumption of integrated circuit to the corresponding clock activities but also suggested by Lim et al. that power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-blocks as well as clock skew across a tributary may be reduced by using a local clock buffer.

2-2. Appellants argue:

"More particularly, there is no motivation to combine the Radjassamy system with Lim, as Radjassamy teaches away from "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Instead, Radjassamy teaches a power consumption correction factor called a "reduction factor"" (page 13, paragraph 3, Appeal Brief)

"As for latch arrays, for example, Radjassamy applies this reduction factor as follows: "the reduction factor may be based on a probabilistic activity profile comprising activity factors that characterize the particular component constraints such as the particular inputs and assertions of the latch array." Radjassamy, Paragraph [0076.] This is clearly a very different approach than "extrapolating energy data by increasing or decreasing the number of active LCBs," as recited in the Claims. Therefore, even if Lim did teach this element, which it does not, Radjassamy clearly rejects it in favor of another approach. For at least this reason, there is no motivation to combine Radjassamy with Lim, and therefore the Examiner's purported prima facie case must fail." (page 14, paragraph 2, Appeal Brief)

The Examiner respectfully disagrees with the Appellants' argument.

Radjassamy discloses at paragraph [0018], "the reduction factor represents a composite probabilistic activity profile associated with each power consumption component that is based on its structural, functional, design and process constraints. Using the *reduction factors for each sub-block*, sub-block level, or portion of the IC of interest, the modified netlist generator 217 provides a modified netlist that *uses a reduced number of components* (e.g., FETs, flip-flops, and the like) to model the portion of the IC of interest as illustrated in further detail in FIG. 4 hereinbelow. Subsequently, the power estimation engine 216 estimates the power consumption based on the modified netlists at the appropriate circuit level, which is essentially a function of a power factor that is modulated by the reduction factors." Using the equation at paragraph [0048] as an example, wherein "F represents the reduction factor for the flip-flops" (paragraph [0055]). "The reduction factor incorporates design-based activity profiles of the flip-flops and may represent a coefficient between 0 and 1 that corrects the worst-case power by taking into considerations such as clock toggling rate and flip-flop toggling rates (paragraph [0056]). It is

well-known that the flip-flops will not change state and will consume minimum power when the clock toggling rate is zero (i.e., clock is inactive). In other words, taking into considerations of clock toggling rate when it is zero, the reduction factor becomes zero representing minimum power consumption of the corresponding flip-flops in a sub-block. Furthermore, Radjassamy suggests that each sub-block may apply its own reduction factor (i.e., taking into considerations of clock toggling rate for each individual sub-block). Therefore, Radjassamy does not teach away as argued by Appellants because via the "reduction factors" of the power consumption equations P_{EST} (energy model), Radjassamy's estimated power consumption of an integrated circuit does comprise extrapolating energy data by the number of active sub-blocks (i.e., the clock toggling rate is not zero).

Lim et al. disclose an apparatus and method for improved clock distribution and control in an integrated circuit having the ability to selectively inhibit clock signals at the local buffer 46. Using inhibit 52 to inhibit the clock at selected locations of the integrated circuit 10 allows for reduction of power dissipation (column 4, lines 62-67). Other features include locally buffered clock signals and multiple clock enables (column 3, lines 33-35). The advantages include reduced delay between buffers and reduced skew across a tributary (column 3, lines 40-42). In other words, Lim et al. suggest power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-blocks as well as clock skew across a tributary may be reduced by using a local clock buffer.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify the reduction factors of the power consumption equations P_{EST} taught by

Radjassamy to incorporate the number of inhibited clock signals at local buffers taught by Lim et al. because, as suggested by Lim et al., power dissipation may be reduced by selectively inhibiting clock signals (i.e., set the clock toggling rate to zero) at the local buffer (i.e., LCB) to essentially have inactive LCBs to reduce the corresponding circuit activities and power dissipation at selected sub-blocks as well as clock skew across a tributary may be reduced by using a local clock buffer.

2-3. Appellants argue:

"The Examiner argues that the above analysis constitutes an impermissible attack of the references individually. Final Action, Page 7 (citing In re Keller, 642 F.2d 413, 2108 USPQ 871 (CCPA 1981); In re Merck & Co., 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986)). Applicants respectfully disagree, in particular as it relates to references that affirmatively teach away from combination with each other, and in other circumstances." (page 14, paragraph 3, Appeal Brief)

"And third, if "the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims prima facie obvious." M.P.E.P. §2143.01(VI) (citing In re Ratti, 270 F.2d 810, 123 USPQ 349 (CCPA 1959)). Applicants respectfully submit that this is just what the Examiner attempts to do in modifying Radjassamy with Lim, as described above. Accordingly, Applicants have not impermissibly attacked the references individually. As such, Applicants respectfully submit that the Examiner's argument fails." (page 15, paragraph 2, Appeal Brief)

The Examiner respectfully disagrees with the Appellants' argument.

As discussed in section **2-2** above, Radjassamy does not teach away as argued by Appellants because via the "reduction factors" of the power consumption equations P_{EST} (energy model), Radjassamy's estimated power consumption of an integrated circuit does comprise

extrapolating energy data by the number of active sub-blocks (i.e., the clock toggling rate is not zero). It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Radjassamy and Lim et al. as detailed in section **2-2** above. Therefore, Appellants' argument against the references individually is not persuasive because one cannot show nonobviousness by attacking references individually where the rejections are based on combinations of references. See *In re Keller*, 642 F.2d 413, 208 USPQ 871 (CCPA 1981); *In re Merck & Co.,* 800 F.2d 1091, 231 USPQ 375 (Fed. Cir. 1986).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Herng-der Day
January 8, 2008

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